TimeLink microsystems

SR1624

IRIGB reader/generator & GPS VME board

PRESENTATION

The board receives time information from two possible sources:

- IRIG B signal: this signal carries the date and time.
- GPS: the information received is the date and hour and the position information's from GPS.

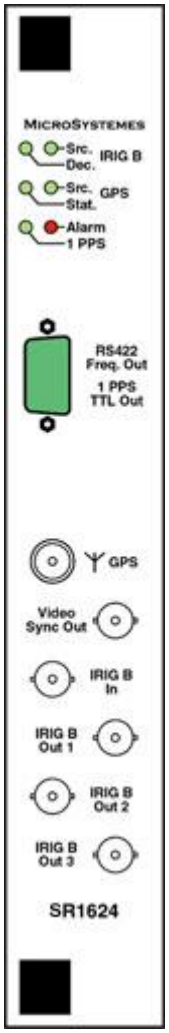
The card is able to delivers time independently in the absence of a source from its internal oscillator.

The board generates signals synchronized to the incoming reference signals:

- 120/240Hz or 100/200 Hz frequency.
- Composite video sync signal CCIR 625 lines/50 Hz standard, NTSC 525 lines/60 Hz.
- IRIG B120 Signal.
- 1PPS Reference signals.

The board is a VME Slave type: A32: A24: A16: D32: D16: D08 (EO), compliant with the revision C of the IEEE 1014 standard. It does not support block transfers.

The board can issue an interrupt on the VME bus each second phased with the 1 PPS. The interrupt level and vector are programmable.



Information's contained in this document are subject to changes without further notice. No responsibility is assumed by TimeLink microsystems for its use. FP0220A- © Copyright TimeLink microsystems.
All rights reserved. www.timelinkmicro.com. Phone: +33 (0)5 62 87 10 70

TimeLink microsystems

SR1624

IRIGB reader/generator & GPS VME board

FUNCTIONALITIES

DESCRIPTION	CHARACTERISTICS
IRIG B code reading	1 KHz carrier, amplitude modulated 1:3 / 1:1 – level 0.5 to 6 V peak-peak. accepted codes: B120, B121, B122, B123 1 PPS accuracy from the read code ± 10 µs, stability ± 1 µs.
GPS receiver dedicated to time applications	Time receiver, 12 channels. Accuracy of 1 PPS: within 15 ns to GPS/UTC (1 Sigma) in fixed position.
Local oscillator (on board)	20 MHz VCXO disciplined with the external reference signals. Stability in free running mode : $\Delta F/F = \pm 5.10^{-6}$ / day Stability in disciplined mode: $\Delta F/F < \pm 1.10^{-9}$ / day
Locking the local 1PPS	Speed of locking: 80 µs/s maximum.
Forced locking of the local 1 PPS at the beginning of the video frame	Selection of the pair or odd frame. This lock causes a time gap in the generated IRIGB frame.
Forced locking of the local 1 PPS on the 1 PPS reference.	This lock causes a time gap in the generated IRIGB frame and in the video synchronisation.
Operating mode	European or US standard selectable by micro-switch.
Frequency output	Reference frequency from the local oscillator: 200 Hz or ~ 239.76 Hz according to the operating mode selected. Possibility of division by 2 to reach 100 Hz or ~119.88 Hz. Signal RS422 compatibles. Signal phased with the local 1 PPS, on the descendant front.
Video sync signal generation	European Standard CCIR 625 lines/50 Hz or US NTSC 525 lines/~59.96 Hz. The beginning of the frame is in advance of 100 ns maximum compared to the local PPS. Output voltage adjustable : Amplitude : from 0.4V to 3.2V
Compatibility mode	The board operates as compatible with the SR1621 VME board or in standard mode. (selectable by micro-switch)

Information's contained in this document are subject to changes without further notice. No responsibility is assumed by TimeLink microsystems for its use. FP0220A- © Copyright TimeLink microsystems.
All rights reserved. www.timelinkmicro.com. Phone: +33 (0)5 62 87 10 70