IRIGB TMC2100 MODULE

USER MANUAL

Reference :	**MN0551**
Release :	**A1**
Date :	**2016-10-27**

CHANGES IN THE DOCUMENT		
Release	**DATE**	**OBJECT of CHANGE**
A1	2016-10-27	Initial version

	Name-Title	**Date and Signature**
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1. GENERAL DESCRIPTION

The TMC2100 IRIGB timing and control module synchronizes PXI systems using GNSS data to perform synchronous events. It features an onboard TCXO that can be disciplined to the GNSS with accuracy better than ±500 ns microsecond for long term stability.

The module provides height independent synchronizations signals routed to PXI TRIG0 to TRIG7 and it also output on the front face an IRIGB signal and programmable RS422 signals.

The module is software controlled via the PCI bus.

1.1. FRONT AND BACK PANELS

The front panel of the equipment includes the following connectors:

- GNSS SMA connector
- RS422 SubD 9 connector.
- IRIGB BR2 connector.

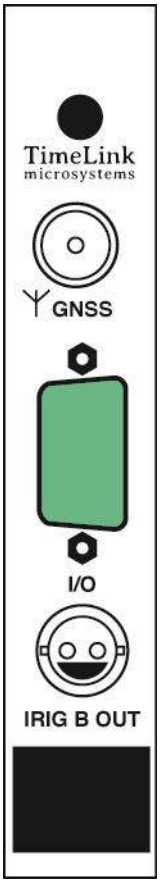


Figure 1 – Front panel

1.2. FUNCTIONAL CHARACTERISTICS

The table below summarizes the functional characteristics of the equipment.

Characteristics	Types/Values
GNSS receiver	GPS + GLONASS bi-constellation integrated receiver
	Female TNC connector for GPS & GLONASS compatible active antenna– 5V or 3.3V power supplied by the receiver.
IRIGB output	BR2 connecter Analog IRIGB (modulation 1:3/1:1, level 0 to 6V peak to peak - 600 Ω)
RS4222 output	Programmable output - Level 0-5V

1.2.1. IRIG B SIGNAL

The IRIGB time is the local time:

Local time = UTC time + UTC offset + time zone + summer/winter time

The generated IRIGB signal is described below:

Pos	Signification	Pos	Signification	Pos	Signification	Pos	Signification	Pos	Signification
0	MARKER REF	1	Second 1	2	Second 2	3	Second 4	4	Second 8
5	0	6	Second 10	7	Second 20	8	Second 40	9	MARKER P1
10	Minute 1	11	Minute 2	12	Minute 4	13	Minute 8	14	0
15	Minute 10	16	Minute 20	17	Minute 40	18	0	19	MARKER P2
20	Hour 1	21	Hour 2	22	Hour 4	23	Hour 8	24	0
25	Hour 10	26	Hour 20	27	0	28	0	29	MARKER P3
30	Day 1	31	Day 2	32	Day 4	33	Day 8	34	0
35	Day 10	36	Day 20	37	Day 40	38	Day 80	39	MARKER P4
40	Day 100	41	Day 200	42	0	43	0	44	0
45	0	46	0	47	0	48	0	49	MARKER P5
50	TD Sign	51	TD Second 1	52	TD Second 2	53	TD Second 4	54	TD Second 8
55	0	56	TD Second 10	57	TD Second 20	58	TD Second 40	59	MARKER P6
60	TD Minute 1	61	TD Minute 2	62	TD Minute 4	63	TD Minute 8	64	0
65	TD Minute 10	66	TD Minute 20	67	TD Minute 40	68	0	69	MARKER P7
70	TD Hour 1	71	TD Hour 2	72	TD Hour 4	73	TD Hour 8	74	0
75	TD Hour 10	76	TD Hour 20	77	0	78	TD Stop	79	MARKER P8
80	0	81	0	82	0	83	0	84	0
85	0	86	0	87	0	88	0	89	MARKER P9
90	0	91	0	92	0	93	0	94	0
95	0	96	0	97		98	0	99	MARKER P0

Note: The TD stop bit is 1 when TD is stopped, 0 when running. TD sign is 1 for negative TD and 0 for positive TD.

1.1.1. RS422 SIGNALS

Four output signals are programmable on the front face RS422; available signals are DCLS, PPS, IRQ, PXI triggers.

1.1.2. PXI SYNCHRONISATION SIGNALS

Height programmable PXI signals are available: TRIG0 to TRIG7. Period and duty cycle are programmable up to 5 MHz. They are synchronized to the general 1 PPS.

2. SOFTWARE CONTROL

This chapter describes how to control the module.

The module is seen as a memory area where control and status registers are defined.

Each register is defined by its relative address to the base address defined by the BIOS at boot or by the operating system.

All registers are 16 or 32 bits, each register access is defined by:

- 'R' : read only access
- 'W': write only access
- 'R/W' : read/write access

2.1. MODULE CONTROL

Address	Access type	Function	Size (bits)
Time TU (Universal Time)			
0x00	R	Status	16
0x02	R/W	Control 1	16
0x04	R/W	Control 2	16
0x08	R	Microsecond meter (0 - 999 999)	32
Time Configuration			
0x10	R/W	Year	16
0x12	R/W	Day of the year (1 to 366)	16
0x14	R/W	Hour (0-23)	16
0x16	R/W	Minute (0-59)	16
0x18	R/W	Second (0-59)	16
Time Count (TD1)			
0x20	R/W	Sign	16

Address	Access type	Function	Size (bits)
0x22	R/W	Hour (0-23)	16
0x24	R/W	Minute (0-59)	16
0x26	R/W	Second (0-59)	16
Time Count (TD2)			
0x30	R/W	Sign	16
0x32	R/W	Hour (0-23)	16
0x34	R/W	Minute (0-59)	16
0x36	R/W	Second (0-59)	16
0x38	R/W	IRIGB level setting B : 0 - 50	16

Note: TD1 and TD2 allow memorizing two TD different values so that an automated reload can be performed. The process is detailed with control register 0x02.

Status register (0x00) :

D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8
ERR	0	0	0	0	0	0	0

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0	0	PHAS	E/H	IRIGB	GNSS	SYNC	ETAT TD

- ERR : 1 = invalid command:

  CHGT TD1, CHGT TD2, CHGT TU avec ETAT TD='1' or START TD='1'.

  Reset by setting bit15 (RAZ ERR) of control register.
- PHAS: 1 = Internal PPS and GNSS PPS phase is better than 500ns
- E/H : 0 = winter time, 1 = summer time
- IRIGB : 0 = not active, 1 = active
- GNSS : 0 = valid GNSS and GNSS 1PPS
- SYNC: 0 = GNSS disciplined, 1 = Not GNSS disciplined
- ETAT TD : 0 = Stop, 1 = Running

Control Register 1 (0x02) :

Read access:

D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8
RAZ ERR	0	0	RAZ_TD	ACT_G	COLD ST	INV IRIG B	VAL E/H

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
TPS GPS	VAL GNSS	VAL IRIGB	CHGT TD2	CHGT TD1	CHGT TU	STOP TD	START TD

- RAZ_ERR: 1 = bit 15 (ERR) reset.
- RAZ_TD: 1 = TD automatically goes from +39:59:59 to +00:00:00 otherwise it sticks to the maximum value.
- ACT_G: 1 = Overall PXI triggers activation.
- COLD ST: 1 = GNSS cold START.
- INV IRIGB: 0 = Standard BR2 IRIGB output signal, BR2, 1 = opposite signal.
- VAL E/H: 0 = no winter/summer hour switch automated management, 1 = automated management
- TPS GPS: 0 = GPS time, 1 = UTC time
- VAL GNSS: 0 = GNSS disabled, 1 = GNSS enabled (when enabled TU is GNSS disciplined).
- VAL IRIGB: 0 = disabled output, 1 = enabled output
- CHGT TD2: 1 = move TD2 content into current T. Only possible when TD is stopped (ETAT TD ='0' et START TD='0').
- CHGT TD1: 1 = move TD1 into current TD. Only possible when TD is stopped (ETAT TD ='0' and START TD='0').
- CHGT TU: 1 = move TU content into current TU. Only possible when TD is stopped (ETAT TD ='0' et START TD='0').
- STOP TD: 1 = Stop time count (TD). This bit is reset at next PPS.
- START TD: 1 = Start time count (TD). This bit is reset at next PPS.

Note: D0 to D4, D15 bits are reset whenever the associated command has been performed.

Read access:

D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8
VAL	0	0	0	0	0	0	0

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0	0	0	0	CD3	CD2	CD1	CD0

- CD3, CD2, CD1, CD0: bit number to be positioned within the register.
- VAL: value of the bit positioned by CD3, CD2, CD1, CD0.

Note: for example to stop TD, write 0x8001 and to load TD2, write 0x8004.

Control register 2 (0x04):

D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8
0	0	0	0	0	0	0	0

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0	0	0	FH SIGN	FH8	FH4	FH2	FH1

- FH SIGN : time zone sign 0 = positive, 1 = negative

- FHx: absolute value of the time zone (binary) 0 to 12.

2.2. CURRENT TIME READING

Current TU and TD matching content of IRIBG signal can be read in the below register. If Data are read right at a second change, they are latched when the year register is accessed; it is unlatched following microsecond register access (register address 0x08) or following a time out if not accessed.

Address	Access	Function	Size (bits)
Time TU (Universal Time)			
0x40	R	Year	16
0x42	R	Day of the year (1 to 366)	16
0x44	R	Hour (0-23)	16
0x46	R	Minute (0-59)	16
0x48	R	Second (0-59)	16
Time Count (TD)			
0x50	R	Sign	16
0x52	R	Hour (0-23)	16
0x54	R	Minute (0-59)	16
0x56	R	Second (0-59)	16

Time count and sign register (0x50):

D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8
0	0	0	0	0	0	0	0

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0	0	0	0	0	0	ETAT	SIGNE

- STATUS : 1 = Stop, 0 = Running
- SIGN : 0 = negative, 1 = positive

2.3. PERIODIC INTERRUPT MANAGEMENT

A periodic interrupt can be generated. The register described below allows defining and activating this interrupt.

Address	Access	Function	Size (bits)
Interrupt Generator			
0x60	R	Status	16
0x62	R/W	Control	16
0x64	R/W	Period	32

Status Register (0x60) :

D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8
0	0	0	0	0	0	0	0

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0	0	0	0	0	0	0	IT

- IT: 1 = an interrupt was triggered. The bit stays high (1) as long as it has not been reset by writing in the control register.

Control register (0x62):

Reading access:

D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8
0	0	0	0	0	0	0	0

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0	0	0	0	0	0	VAL_IT	RST_IT

- VAL_IT: 0 = interrupt not transmitted, 1 = interrupt transmitted.
- RST_IT: 1 = interrupt reset command

Writing access:

D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8
VAL	0	0	0	0	0	0	0

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0	0	0	0	0	CD2	CD1	CD0

- CD3, CD2, CD1, CD0: bit number to be positioned within the register.
- VAL: value of the bit positioned by CD3, CD2, CD1, CD0 (usually 1).

Note: to reset the interrupt, write 0x8000 and to activate it write 0x8001.

Period Register (0x64):

The period value is the time interval between two interrupts. Time is defined by multiple of 100ns, minimum value is 10000 (1ms). The interrupt is synchronized on the 1 PPS.

2.4. VERSION INFORMATION

Version information is available in the register described below.

Address	Access	Function	Size (bits)
Interrupt Generator			

Address	Access	Function	Size (bits)
0x70 to 0x7F	R	Characters hardware version terminated by zero (Ex : ATxxxxyy)	16 x 8
0x80 to 0x8F	R/W	Characters software version terminated by zero (Ex : LOxxxxyy)	16 x 8

2.5. FREQUENCY GENERATOR

Height frequency generators are available. They are programmed via the register described below:

Address	Access	Function	Size (bits)
Frequency generator 1			
0x152	R/W	Control	16
0x154	R/W	Period	32
0x158	R/W	TimeON	32
Frequency generator 2			
0x162	R/W	Control	16
0x164	R/W	Period	32
0x168	R/W	TimeON	32
Frequency generator 3			
0x172	R/W	Control	16
0x174	R/W	Period	32
0x178	R/W	TimeON	32
Frequency generator 4			
0x182	R/W	Control	16
0x184	R/W	Period	32
0x188	R/W	TimeON	32
Frequency generator 5			
0x192	R/W	Control	16
0x194	R/W	Period	32
0x198	R/W	TimeON	32
Frequency generator 6			
0x1A2	R/W	Control	16
0x1A4	R/W	Period	32
0x1A8	R/W	TimeON	32
Frequency generator 7			
0x1B2	R/W	Control	16
0x1B4	R/W	Period	32

Address	Access	Function	Size (bits)
0x1B8	R/W	TimeON	32
Frequency generator 8			
0x1C2	R/W	Control	16
0x1C4	R/W	Period	32
0x1C8	R/W	TimeON	32

Control register (0x92, 0x9A, 0xA2, 0xAA, 0xB2, 0xBA, 0xC2, 0xCA) :

Reading access / writing:

D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8
0	0	0	0	0	0	0	0

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
0	0	0	0	ACT SYNC	TRISTATE	INV	ACT LOC

- TRISTATE: high impedance setting.
- INV: 0 = rising edge synchronized to 1 PPS, 1 = opposite signal.
- ACT LOC: 1 = signal is triggered by next PPS rising edge.
- ACT SYNC: 1 = signal is triggered by next PPS rising edge if « ACT_G » control register bit is set. It allows to group TRIG pin within a single synchronization

TRIGS state before internal PPS triggering:

TRISTATE	ACT	INV	TRIG level
0	0	X	HIGHZ
0	1	X	HIGHZ
1	X	0	0
1	X	1	1

TRIGS state after internal PPS triggering:

TRISTATE	ACT	INV	TRIG level
0	0	X	HIGHZ
1	0	0	0
1	0	1	1
X	1	0	FREQ
X	1	1	Inverted FREQ

ACT = ACT_LOCAL '**or**' (ACT_SYNC '**and**' ACT_G)

Period register (0x1X4) :

The period value is the time interval between two interrupts. Time is defined by multiple of 100ns.

TimeON Register (0x1X8) :

This register value set the time the signal is high (1). It is defined by multiple of 100ns.

Signal frequency	Period Value	TimeON	Duty cycle
1 KHz	10000	1000	10 %
200 KHz	50	25	50 %
250 KHz	40	36	90 %

2.6. SUMMER/WINTER TIME INFORMATIONS

Data to control summer/winter time switch are available within the below registers.

Address	Access	Function	Size (bits)
0xD0	R/W	Second count since 1/01/1970 matching start of summer time	32
0xD8	R/W	Second count since 1/01/1970 matching start of winter time	32

Data are calculated within the example program daylight.c

2.7. GNSS DATA

GNSS receiver data are available within the register described below.

Address	Access	Function	Size (bits)
GNSS receiver data			
0x100	R	Status	16
0x102		*Not used*	16
0x104	R	Second (0-59)	16
0x106	R	Minute (0-59)	16
0x108	R	Hour (0-23)	16
0x10A	R	Day of the year (1-366)	16
0x10C	R	Year	16
0x10E	R	Month (1-12)	16
0x110	R	Day of the months (1-31)	16
0x112	R	Day of the week (0-6 ; Sunday = 0)	16

Address	Access	Function		Size (bits)
0x114	R	Latitude (radians, + north, - south)		32
0x118	R	Longitude (radians, + east, - west)		32
0x11C	R	Altitude (meter)		32
0x120	R	Satellite count		16
0x122	R	ID satellite 1	ID satellite 2	16
0x124	R	ID satellite 3	ID satellite 4	16
0x126	R	ID satellite 5	ID satellite 6	16
0x128	R	ID satellite 7	ID satellite 8	16
0x12A	R	ID satellite 9	ID satellite 10	16
0x12C	R	ID satellite 11	ID satellite 12	16
0x12E	R	ID satellite 13	ID satellite 14	16
0x130	R	ID satellite 15	ID satellite 16	16
0x132	R	UTC Offset		16

2.8. RS422 SIGNALS CONFIGURATION

Address	Access	Function	Size (bits)
DB9 Configuration			
0xE0	R/W	Output 1 Configuration (+pin1 -pin6)	8
0xE1	R/W	Output 1 Configuration (+pin2 –pin7)	8
0xE2	R/W	Output 1 Configuration (+pin3 –pin8)	8
0xE3	R/W	Output 1 Configuration (+pin4 –pin9)	8

Value to write	Selected signal
0, 1, 2	GND
3	VCC
4	IRIG B DCLS
5	Internal PPS
6	GNSS PPS
7	IRQ
8 to 15	PCI triggers

2.9. LINUX DRIVER MODULE CONTROL

The module is controlled by software via a driver which controls directly the different registers. The driver mainly uses ioctl system function. Below are listed the main standard Linux driver function.

Note: The data structure is defined within the provided file tmc2100.h.

Function	Description	Comment
`open()`	Open driver.	To be called first

Function	Description	Comment
`close()`	Close driver.	To be called last.
`read()`	Current time value and global status register reading.	If read() is done in non blocking mode, it returns the current time value. If read() is done in blocking mode, the time reading is synchronized to the periodic interrupt
`ioctl(TMC2100_RESET_INT)`	Interrupt reset	Clear and disable periodic interrupt
`ioctl(TMC2100_VERSION, &version)`	Embedded FPGA and firmware version reading.	
`ioctl(TMC2100_STATUS, &status)`	Status registers reading (0x00).	
`ioctl(TMC2100_CONTROL1, &control)`	N°1 control register writing	
`ioctl(TMC2100_SET_TZ)`	Time zone update.	+/-12 h
`ioctl(TMC2100_SET_FREQ, &freq_struct)`	Frequency generator N configuration.	N = 0 à 7.
`ioctl(TMC2100_GET_FREQ, &freq_struct)`	Frequency generator N registers reading.	N = 0 à 7.
`ioctl(TMC2100_SET_INT, &period)`	Activate the periodic interrupt.	Period is a multiple of 100ns. Minimum value is 1ms
`ioctl(TMC2100_GET_INT, &val)`	Periodic interrupt register reading.	
`ioctl(TMC2100_LOAD_TD1, &td_struct)`	TD1 loading.	
`ioctl(TMC2100_LOAD_TD2, &td_struct)`	TD2 loading.	
`ioctl(TMC2100_RESET_TD)`	TD is loaded with TD2 value	
`ioctl(TMC2100_START_TD)`	Start time count from current value.	
`ioctl(TMC2100_STOP_TD)`	Stop time count at current value.	
`ioctl(TMC2100_SET_TIME)`	Manual time setup.	Available only if GNSS is disabled or not valid
`ioctl(TMC2100_GET_GNSS, &gnss_struct)`	GNSS register reading.	
`ioctl(TMC2100_DUMP, &buffer)`	Module memory dump.	Debug purpose
`ioctl(TMC2100_SET_LEVEL)`	Set output signal level.	
`ioctl(TMC2100_DAYLIGHT, &daylight_struct)`	Set start and end of summer and winter time.	

SAMPLE PROGRAMMES

Sample programs showing how to use the different functions are provided

Program	Description
`control <bit number> <value>`	Set a bit within the control register 1. <Bit number> = 0 à 7.

Program	Description
`currenttime`	Time reading (non blocking mode).
`daylight <year>`	Calculate summer and winter start time of the specified year and write it in the associated registers.
`dump`	Dump the module memory.
`getfreq <channel>`	Frequency generator parameters reading <channel> (0 à 7).
`gnss`	GNSS current data reading.
`inittime`	Set date and time to « 2016 001 12 :30 :15 ».
`loadtd <reg> ±HH:MM:SS`	TD1 and 2 loading (<reg> = 1 for TD1 and 2 for TD2)
`periodic [<interval ms>]`	Time reading interrupt mode (default period if not set = 1ms)
`reset`	Periodic interrupt disabled.
`setfreq <channel> <active> [<invert> <divisor>]`	Frequency generator programming <channel> (0 à 7). <active> = 1 to enable and 0 to disable. <invert> = 1 to invert. <divisor> = 10 MHz clock divider.
`setlevel <value>`	IRIG B output signal level: 0 à 50.
`status`	Display status and control 1 registers.
`tdreset`	Load TD2 value in current TD
`tdstart`	Start TD
`tdstop`	Stop TD
`timezone ±HH`	Set the time zone
`version`	Display FPGA and firmware version.

3. GETTING STARTED

3.1. CONNECTIONS

The following connections must be made:

- Insert the module into the PXI rack.
- Connect the GNSS antenna cable to the antenna input of the equipment.
- Connect the output signals if needed.

3.2. POWERING UP

The module starts when the power is applied to the unit. There is no ON/OFF switch.

3.3. MODULE PC CONTROL SOFTWARE

The module comes with a set of software including sample software. This software requires a Linux system with a kernel above version 2.6. It includes:

- A driver located into the /tmc2100 to be compiled on the targeted system
- A set of sample application files located into /tmc2100/interface demonstrating how to control the driver

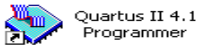
4. MAINTENANCE

Maintenance operations are limited to firmware update.

4.1. PREREQUISITE

- A 32 or 64 bits Windows PC
- A mini-USB cable
- The provided upgrade firmware

4.2. HOW TO PROCEED

- Quartus Programmer software install
- USB-Blaster driver install
- Connect the min-USB cable to the module
- Run 

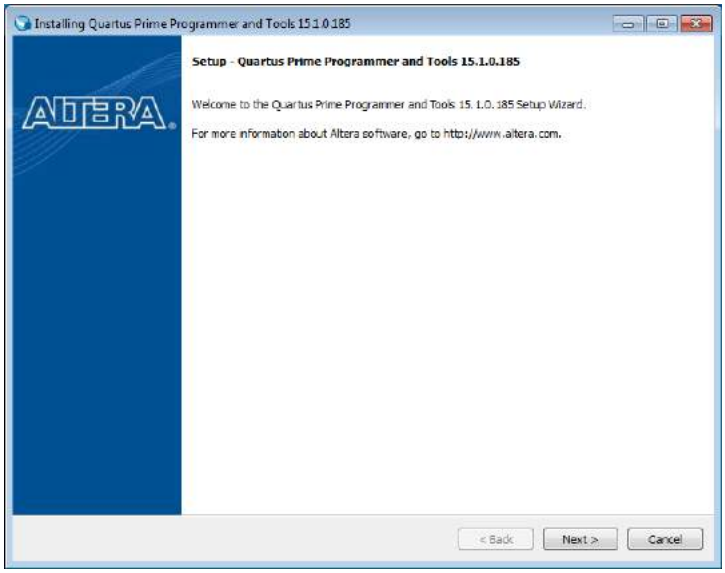
4.2.1. QUARTUS PROGRAMMER SOFTWARE INSTALL

Install either (available for downloading):

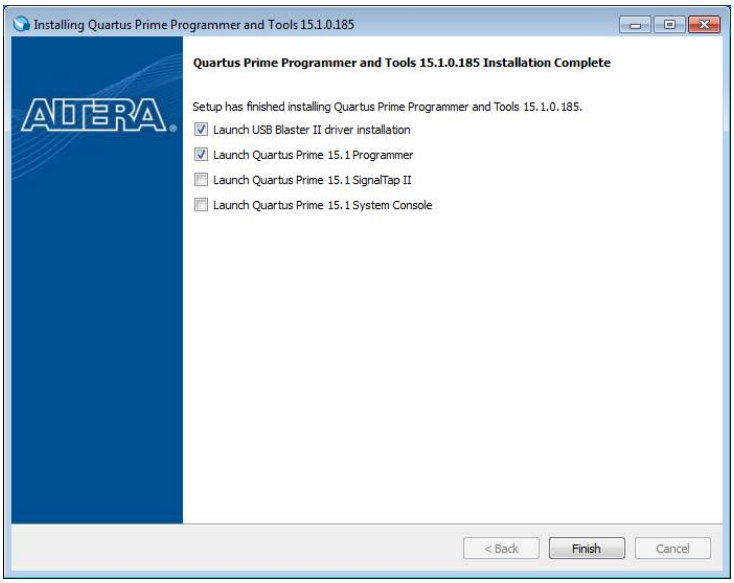
QuartusProgrammerSetup-15.1.0.185-windows32.exe

Or

QuartusProgrammerSetup-15.1.0.185-windows64.exe

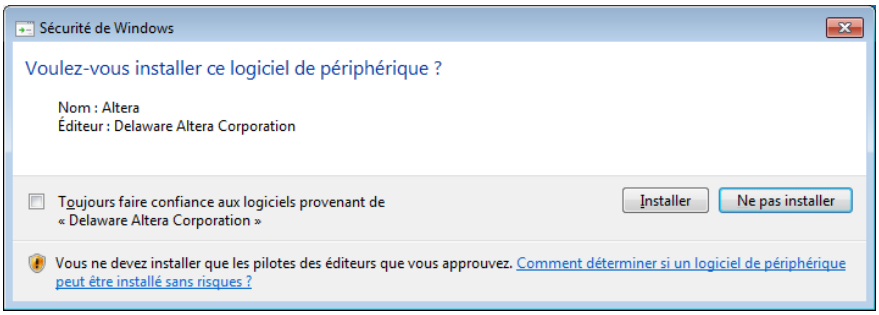


Click next until:

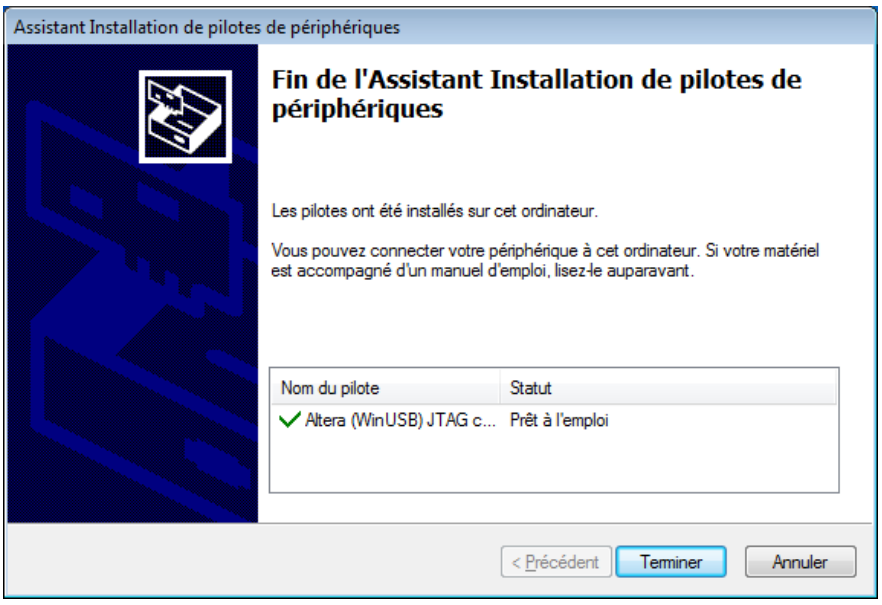


Select first 2 options.

4.2.2. USB-BLASTER DRIVER INSTALL



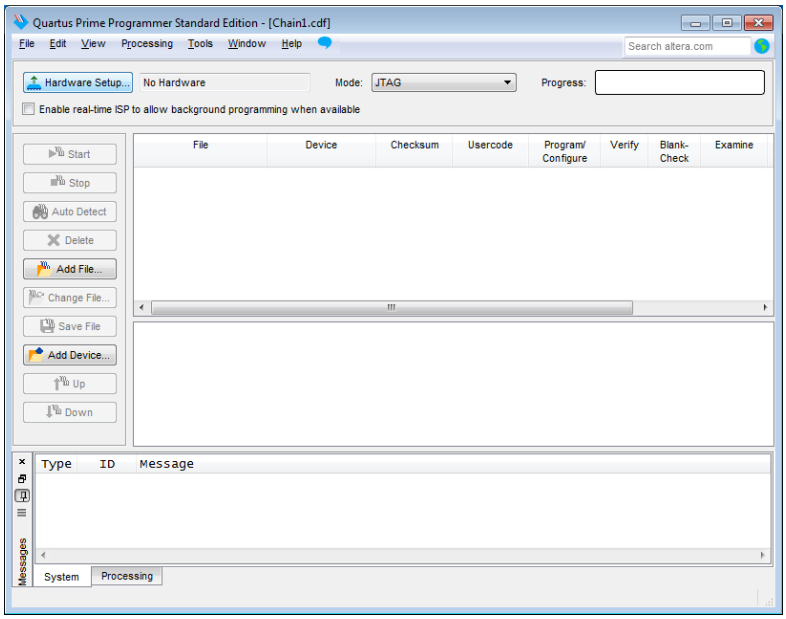
Click on INSTALL



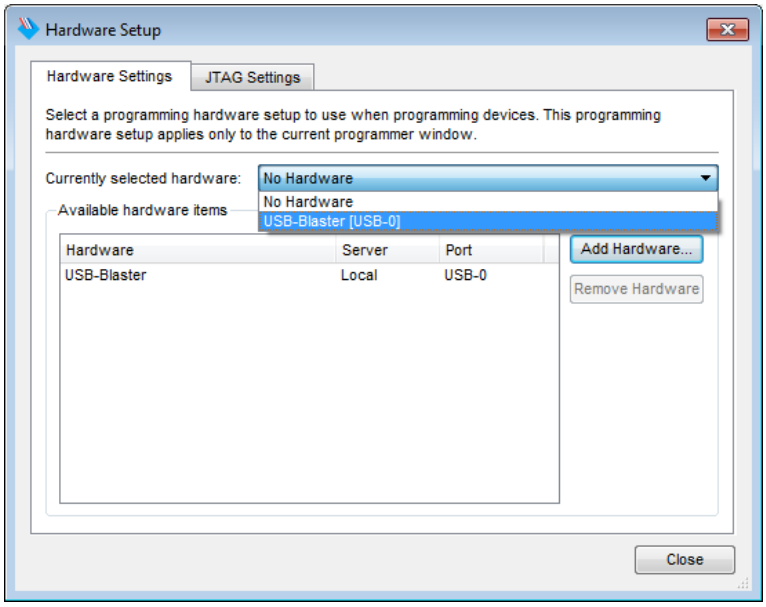
Connect the module (outside the rack) to the PC using the mini-USB cable. The module is power supplied by the USB. Click on Terminate.

4.3. DOWNLOAD

Run the download tool



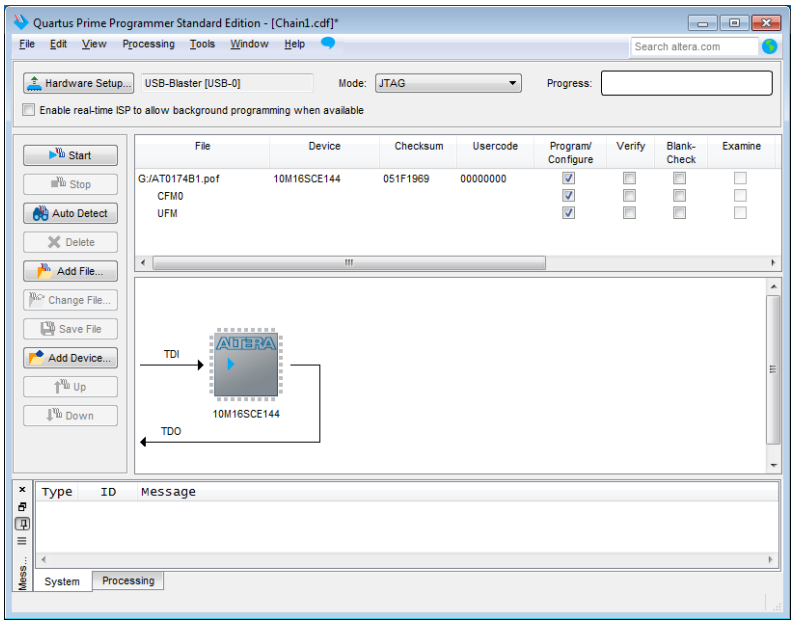
If « No hardware » is displayed click « hardware setup »



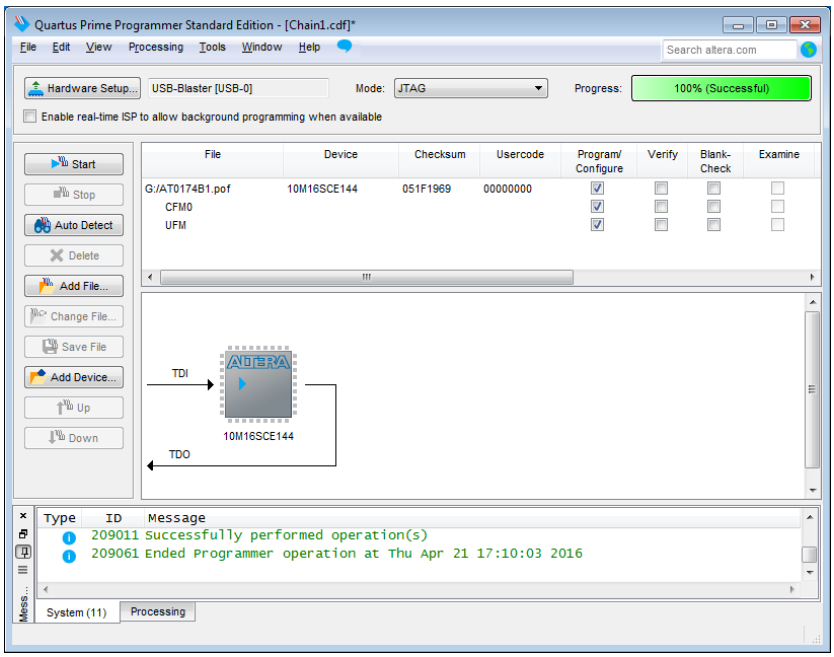
Select « USB-Blaster [USB-0] »

If the accessory does not display, close the window and click again on « hardware setup »

Click « add file » and select the file « ATXXXX.POF »



Select the 3 radio buttons « Program/configure » and click « start »



Download is done.

Disconnect the USB cable.

*** End of document ***